REMARKS

Reconsideration of the present application is respectfully requested.

Claims 4 and 5 have been canceled without prejudice or disclaimer in view of the election of claims 1-3 and 6 in the Response to Restriction Requirement filed on April 27, 2004. Applicants expressly reserve the right to file a divisional application on these claims at any time during the pendency of the present application.

The Examiner has rejected claims 1, 2 and 6 under 35 USC 103(a) as being obvious in view of the combination of Yamasaki and Nakajima. This rejection is respectfully traversed.

Claims 1, 2 and 6 have been amended to generally recite that a microcomputer is immediately reset when voltages from power sources are not within specified ranges or are not below specified voltages. Support for these amendments may be found, for example, on page 19, line 23 – page 20, line 1 and page 25, lines 9-12.

The Examiner asserts that, while Yamasaki does not teach or suggest resetting a microcomputer when a voltage abnormality is detected, Nakajima cures this deficiency by teaching resetting of a microcomputer when a voltage supplied to the microcomputer falls below, and remains below, a normal level for a predetermined period of time.

However, Nakajima neither teaches nor suggests resetting the microcomputer immediately when the supplied voltages from power sources are not within specified ranges or are not below specified voltages as now generally recited in claims 1, 2 and 6. Rather, as noted above, the reset circuit in Nakajima resets a microcomputer when a voltage supplied to the microcomputer falls below, and remains below, a normal level for a predetermined period of time. In fact, Nakajima actually teaches away from immediately resetting a microcomputer, as the above mentioned delay is designed to

avoid resetting of a programmed operation every time a first power source is cut off instantaneously (See col. 2, lines 52-57of Nakajima.)

Therefore, as the combination of Yamasaki and Nakajima does not render the present invention as recited in claims 1, 2 and 6 obvious, it is respectfully requested that the Examiner's rejection of these claims under 35 USC 103(a) be withdrawn.

The Examiner has rejected claim 3 under 35 USC 103(a) as being obvious in view of the combination of Yamasaki, Nakajima and Carter. This rejection is respectfully traversed.

Yamasaki and Nakajima are inapplicable for the above discussed reasons. The Examiner asserts that Carter teaches detecting if current being input to a computer deviates from a predetermined range.

However, Carter neither teaches nor suggests resetting the microcomputer immediately when the supplied voltages from power sources are not within specified ranges or are not below specified voltages as now generally recited in claim 1 from which claim 3 depends. In addition, Carter does not teach or suggest resetting a computer immediately when any one of the currents flowing into first and second power output circuits are detected as being outside first and second specified ranges.

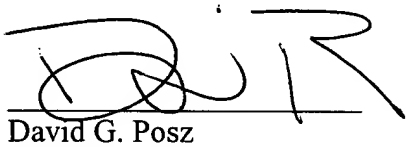
Therefore, as the combination of Yamasaki, Nakajima and Carter does not render the present invention as recited in claim 3 obvious, it is respectfully requested that the Examiner's rejection of claim 3 under 35 USC 103(a) be withdrawn.

Claim 7 has been added and recites an electronic control apparatus including *inter alia* a reset control circuit for immediately resetting a microcomputer in response to an

abnormality signal generated by either of first and second abnormality detection circuits. This feature is supported at, for example, page 25, lines 9-12 of the specification.

In view of the above remarks, the present application is believed to be in condition for allowance. A prompt notice to that effect is respectfully requested. Although no fees are believed to be due, permission is hereby given to charge any unforeseen fees to deposit account 50-1147.

Respectfully submitted,



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